REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																					
PAGE																					
REV																					
PAGE																					
REV STATUS OF PAGES	**REV**																				
	PAGE	1	2	3	4	5	6	7	8	9	10	11	12	13							

PMIC N/A	**PREPARED BY** Phu H. Nguyen	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** **http://www.landandmaritime.dla.mil/**
Original date of drawing YY MM DD 12-10-23	**CHECKED BY** Phu H. Nguyen **APPROVED BY** Thomas M. Hess	**TITLE** MICROCIRCUIT, DIGITAL-LINEAR, CMOS, 170 MHz, TRIPLE, 10-BIT HIGH SPEED VIDEO DAC, MONOLITHIC SILICON
	SIZE A / **CODE IDENT. NO.** 16236	**DWG NO.** **V62/12637**
	REV	**PAGE** 1 **OF** 13

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance CMOS, 170 MHz, triple, 10-bit high speed video DAC, microcircuit, with an operating temperature range of -55°C to +105°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/12637	-	01	X	B
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	ADV7123-EP	CMOS, 170 MHz, triple, 10-bit high speed video DAC

1.2.2 Case outline(s). The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	10	JEDEC MO-220-WKKD	Lead Frame Chip Scale Package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/ 2/

V_{AA} to GND	+7.0 V
Voltage on any digital pin	GND – 0.5 V to V_{AA} + 0.5 V
I_{OUT} to GND	0 V to V_{AA} 2/
Ambient operating temperature (T_A)	-55°C to +105°C
Storage temperature (T_S)	-65°C to 150°C
Junction temperature (T_J)	150°C
Lead temperature,(Soldering, 10 sec)	300°C
Vapor phase Soldering (1 minute)	220°C

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at http:/www.jedec.org or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3 and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Terminal function. The terminal function shall be as shown in figure 3.

3.5.4 Functional block diagram. The functional block diagram shall be as shown in figure 4.

3.5.5 Timing diagram. The timing diagram shall be as shown in figure 5.

1/ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

2/ Analog outputs short circuit to any power supply or common GND can be of an indefinite duration.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Test conditions 2/	Limits			Unit
			Min	Typ	Max	
Static performance						
Resolution (Each DAC)		R_{SET} = 680 Ω			10	Bits
Integral nonlinearity (BSL)			-1	+0.5	+1	LSB
Differential nonlinearity			-1	+0.25	+1	
Digital and control inputs						
Input high voltage	V_{IH}		2.0			V
Input low voltage	V_{IL}			0.8		
Input current	I_{IN}		-1		+1	µA
$\overline{PSAVE}$ pull up current				20		
Input capacitance	C_{IN}			10		pF
Analog outputs						
Output current		Green DAC, $\overline{SYNC}$ = high	2.0		26.5	mA
		RGB DAC, $\overline{SYNC}$ = low	2.0		18.5	
DAC to DAC matching				1.0		%
Output compliance Range	V_{OC}		0		1.4	V
Output impedance	R_{OUT}			70		kΩ
Output capacitance	C_{OUT}			10		pF
Offset error		Tested with DAC output = 0 V		0	0	%FSR
Gain error 4/		FSR = 17.62 mA		0		
Voltage reference, external						
Reference range	V_{REF}		1.12	1.235	1.35	V
Voltage reference, internal						
Reference range	V_{REF}			1.235		V
Power dissipation						
Digital supply current 5/		f_{CLK} = 50 MHz		2.2	5.0	mA
		f_{CLK} = 140 MHz		6.5	12.0	
		f_{CLK} = 517 MHz		7.5	13.5	
Analog supply current		R_{SET} = 680 Ω		67	72	
		R_{SET} = 680 Ω		8		
Standby supply current		$\overline{PSAVE}$ = low, digital and control inputs at V_{DD}		2.1	5.0	
Power supply rejection ratio				0.1	0.5	%/%

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions 6/	Limits			Unit
			Min	Typ	Max	
DYNAMIC SPECIFICATIONS						
AC LINEARITY 3/						
Spurious free Dynamic Range to Nyquist 7/						
Single ended output						
f_{CLK} = 50 MHz, f_{OUT} = 1.00 MHz				67		dBc
f_{CLK} = 50 MHz, f_{OUT} = 2.51 MHz				67		
f_{CLK} = 50 MHz, f_{OUT} = 5.04 MHz				63		
f_{CLK} = 50 MHz, f_{OUT} = 20.2 MHz				55		
f_{CLK} = 100 MHz, f_{OUT} = 2.51 MHz				62		
f_{CLK} = 100 MHz, f_{OUT} = 5.04 MHz				60		
f_{CLK} = 100 MHz, f_{OUT} = 20.2 MHz				54		
f_{CLK} = 100 MHz, f_{OUT} = 40.4 MHz				48		
f_{CLK} = 140 MHz, f_{OUT} = 2.51 MHz				57		
f_{CLK} = 140 MHz, f_{OUT} = 5.04 MHz				58		
f_{CLK} = 140 MHz, f_{OUT} = 20.2 MHz				52		
f_{CLK} = 140 MHz, f_{OUT} = 40.4 MHz				41		
Double ended output						
f_{CLK} = 50 MHz, f_{OUT} = 1.00 MHz				70		dBc
f_{CLK} = 50 MHz, f_{OUT} = 2.51 MHz				70		
f_{CLK} = 50 MHz, f_{OUT} = 5.04 MHz				65		
f_{CLK} = 50 MHz, f_{OUT} = 20.2 MHz				54		
f_{CLK} = 100 MHz, f_{OUT} = 2.51 MHz				67		
f_{CLK} = 100 MHz, f_{OUT} = 5.04 MHz				63		
f_{CLK} = 100 MHz, f_{OUT} = 20.2 MHz				58		
f_{CLK} = 100 MHz, f_{OUT} = 40.4 MHz				52		
f_{CLK} = 140 MHz, f_{OUT} = 2.51 MHz				62		
f_{CLK} = 140 MHz, f_{OUT} = 5.04 MHz				61		
f_{CLK} = 140 MHz, f_{OUT} = 20.2 MHz				55		
f_{CLK} = 140 MHz, f_{OUT} = 40.4 MHz				53		
Spurious free Dynamic Range within a window						
Single ended output						
f_{CLK} = 50 MHz, f_{OUT} = 1.00 MHz; 1 MHz Span				77		dBc
f_{CLK} = 50 MHz, f_{OUT} = 5.04 MHz; 2 MHz Span				73		
f_{CLK} = 140 MHz, f_{OUT} = 5.04 MHz; 4 MHz Span				64		
Double ended output						
f_{CLK} = 50 MHz, f_{OUT} = 1.00 MHz; 1 MHz Span				74		dBc
f_{CLK} = 50 MHz, f_{OUT} = 5.04 MHz; 2 MHz Span				73		
f_{CLK} = 140 MHz, f_{OUT} = 5.04 MHz; 4 MHz Span				60		

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions 6/	Limits			Unit
			Min	Typ	Max	
DYNAMIC SPECIFICATIONS – Continued.						
AC LINEARITY – Continued. 3/						
Total harmonic distortion						
f_{CLK} = 50 MHz, f_{OUT} = 1.00 MHz						
T_A = 25°C				66		dBc
-55°C ≤ T_A ≤ +105°C				65		
f_{CLK} = 50 MHz, f_{OUT} = 2.00 MHz				64		
f_{CLK} = 100 MHz, f_{OUT} = 2.00 MHz				64		
f_{CLK} = 140 MHz, f_{OUT} = 2.00 MHz				55		
DAC performance						
Glitsh impulse				10		pV-sec
DAC to DAC crosstalk 8/				23		dB
Data feedthrough 9/ 10/				22		dB
Clock feddthrough 9/ 10/				33		dB

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions 2/	Limits			Unit
			Min	Typ	Max	
TIMING SPECIFICATIONS 3/ 11/						
Analog outputs						
Analog output delay	t_6			7.5		ns
Analog output Rise/Fall time 12/	t_7			1.0		
Analog output transition time 13/	t_8			15		
Analog output skew 14	t_9			1	2	
Clock control						
Clock frequency 15/	f_{CLK}				170	MHz
Data and control setup	t_1		0.68			ns
Data and control hold	t_2		2.9			
Clock period	t_3		5.88			
Clock pulse width high 14/	t_4	$f_{CLK\ MAX}$ = 170 MHz	2.6			
Clock pulse width low 14/	t_5	$f_{CLK\ MAX}$ = 170 MHz	2.6			
Pipeline delay 14/	t_{PD}		1.0	1.0	1.0	Clock cycles
$\overline{\text{PSAVE}}$ up time 14/	t_{10}			4	10	ns

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ V_{AA} = 3.0 V to 3.6 V, V_{REF} = 1.235 V, R_{SET} = 560 Ω, C_L = 10 pF, -55°C ≤ T_A ≤ +105°C , unless otherwise noted; $T_{J\ MAX}$ = 110°C.

3/ These maximum/minimum specifications are guaranteed by characterization over the 3.0 V to 3.6 V range.

4/ Gain error = {Measured (FSC)/Ideal (FSC) – 1) X 100}, where ideal (FSC) = V_{REF}/R_{SET} X K X (0x3FFH) and K = 7.9896.

5/ Digital supply is measured with a continuous clock that has data input corresponding to a ramp pattern and with an input level at 0 V and V_{DD}.

6/ V_{AA} = 3.0 V to 3.6 V, V_{REF} = 1.235 V, R_{SET} = 680 Ω, C_L = 10 pF. All specifications are at T_A = 25°C, unless otherwise noted; $T_{J\ MAX}$ = 110°C.

7/ This device exhibits high performance when operating with an internal voltage reference, V_{REF}.

8/ DAC to DAC crosstalk measured by holding one DAC high while the other two DAC are making low to high and high to low transactions.

9/ Clock and data feedthrough is a function of the amount of overshoot and undershoot on the digital inputs. Glitch impulse includes clock and data feedthrough.

10/ TTL input values are 0 V to 3 V, with input rise/Fall times of 3 ns, measured at the 10% and 90% points. Timing reference points are 50% for inputs and outputs.

11/ Timing specifications are measured with input levels of 3.0 V (V_{IH}) and 0 V (V_{IL}).

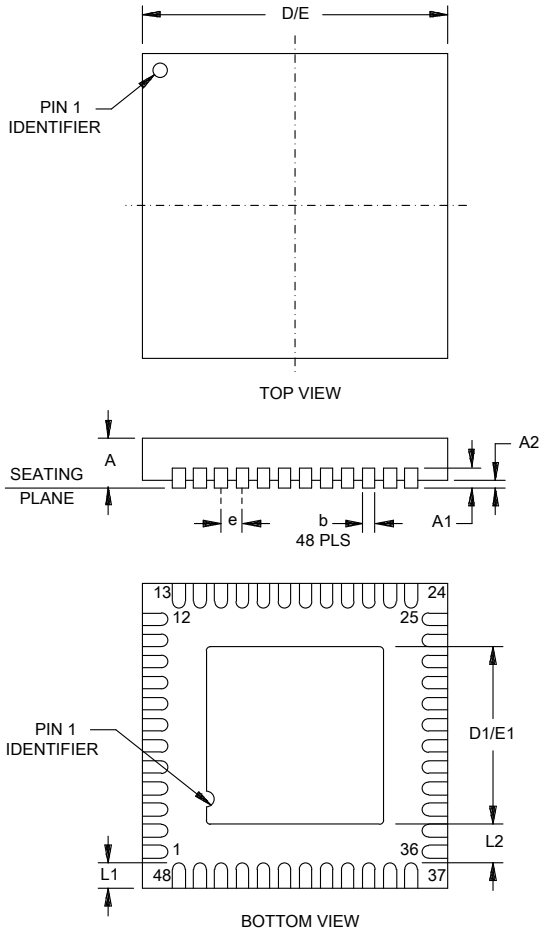
12/ Rise time was measured from the 10% and 90% point of zero full scale transition, fall time from 90% to 10% point of a full scale transition.

13/ Measured from the 50% point of full scale transition to within 2% of the final output value.

14/ Guaranteed by characterization.

15/ f_{CLK} maximum specification production tested at 125 MHz.

Case X



Dimensions					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A	0.70	0.80	D1/E1	3.95	4.25
A1	0.20 REF		e	0.50 BSC	
A2		0.05	L1	0.35	0.45
b	0.18	0.30	L2	0.25	
D/E	7.00 BSC				

NOTES:
1. All linear dimensions are in millimeters.
2. Falls within JEDEC MO-220-WKKD.

FIGURE 1. Case outline.

Case outline X

Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	G0	25	GND
2	G1	26	GND
3	G2	27	$\overline{\text{IOB}}$
4	G3	28	IOB
5	G4	29	V_{AA}
6	G5	30	V_{AA}
7	G6	31	$\overline{\text{IOG}}$
8	G7	32	IOG
9	G8	33	$\overline{\text{IOR}}$
10	G9	34	IOG
11	$\overline{\text{BLANK}}$	35	COMP
12	$\overline{\text{SYNC}}$	36	V_{REF}
13	V_{AA}	37	R_{SET}
14	B0	38	$\overline{\text{PSAVE}}$
15	B1	39	R0
16	B2	40	R1
17	B3	41	R2
18	B4	42	R3
19	B5	43	R4
20	B6	44	R5
21	B7	45	R6
22	B8	46	R7
23	B9	47	R8
24	CLOCK	48	R9

FIGURE 2. Terminal connections.

Case outline X.

Terminal		Description
Number	Mnemonic	
1 to 10	IN1	Red, Green, and Blue pixel data inputs (TTL compatible). Pixel data is latched on the rising edge of clock. R0, G0, and B0 are the least significant data bits. Unused pixel data inputs should be connected to either the regular printed circuit board (PCB) power or ground plate.
14 to 23	D1	
39 to 48	S1	
11	$\overline{\text{BLANK}}$	Composite Blank Control input (TTL compatible). A logic 0 on this control input drives the analog outputs – IOR, IOB, and IOG – to the blanking level. The $\overline{\text{BLANK}}$ signal is latched on the rising edge of CLOCK. When $\overline{\text{BLANK}}$ is a logic 0, the R0 to R9, G0 to G9, and B0 to B9 pixel inputs are ignored.
12	$\overline{\text{SYNC}}$	Composite Sync Control input (TTL compatible). A logic 0 on the $\overline{\text{SYNC}}$ input switches off a 40 IRE current source. The sync current is internally connected to the IOG analog output. $\overline{\text{SYNC}}$ does not override any other control or data input; therefore, it should only be asserted during the blanking interval. $\overline{\text{SYNC}}$ is latched on the rising edge of CLOCK. If sync information is not required on the green channel, the $\overline{\text{SYNC}}$ input should be tied to logic 0.
13, 29, 30	V_{AA}	Analog Power supply (3.3 V ±10%). All V_{AA} pins on this device must be connected.
24	CLOCK	Clock Input (TTL compatible). The rising edge of CLOCK latched at the R0 to R9, G0 to G9, B0 to B9. $\overline{\text{SYNC}}$, and $\overline{\text{BLANK}}$ pixel and control inputs. Typically, the CLOCK input is the pixel clock rate of the video system. CLOCK should be driven by a dedicated TTL buffer.
25, 26	GND	Ground. The GND pins must be connected.
27, 31, 33	$\overline{\text{IOB}}$, $\overline{\text{IOG}}$, $\overline{\text{IOR}}$	Differential Red, Green, and Blue current outputs (High impedance current sources). These RGB video outputs are specified to directly drive RS-343A and RS-170 video levels into a doubly terminated 75 Ω coaxial cable. If the complementary outputs are not required, these outputs should be tie to ground.
28, 32, 34	IOB, IOG, IOR	Red, Green and Blue current outputs (High impedance current sources) . These RGB video outputs are specified to specified to directly drive RS-343A and RS-170 video levels into a doubly terminated 75 Ω coaxial cable. All three currents outputs should have similar output loads whether or not they are all being used.
35	COMP	Compensation pin for the Internal Reference Amplifier. A 0.1 µF ceramic capacitor must e connected between COMP and V_{AA}.
36	V_{REF}	Voltage Reference Input for DACs or Voltage Reference Output (1.235 V). The V_{REF} pin is normally terminated to V_{AA} through a 0.1 µF capacitor. However, this device can be overdriven by an external 1.23 V reference (AD1580), if required.
37	R_{SET}	A resistor (R_{SET}) connected between this pin and GND controls the magnitude of the full scale video signal. Note that the IRE relationships are maintained, regardless of the full scale output current. For nominal video levels into a doubly terminated 75 Ω load, R_{SET} = 530 Ω. The relationship between R_{SET} and the full scale output current on IOG (assuming I_{SYNC} is connected to IOG) is given by: R_{SET} (Ω) = 11,445 X V_{REF} (V)/IOG (mA) The relationship between R_{SET} and the full scale output current on IOR, IOG and IOB is given by: IOG (mA) = 11,445 X V_{REF} (V)/RSET (Ω) ($\overline{\text{SYNC}}$ being asserted) IOR, IOB (mA) = 7989.6 X V_{REF} (V)/R_{SET} (Ω) The equation for IOG is the same as that for IOR and IOB when $\overline{\text{SYNC}}$ is not being used, that is, $\overline{\text{SYNC}}$ is tied permanently low.
38	$\overline{\text{PSAVE}}$	Power Save Control pin. Reduce power consumption is available on this device when this pin is active.
EP	Exposed Pad	The exposed paddle on the underside of the package must be soldered to the ground plane to increase the reliability of the solder joints and to the maximize the thermal capability of the package.

FIGURE 3. Terminal function.

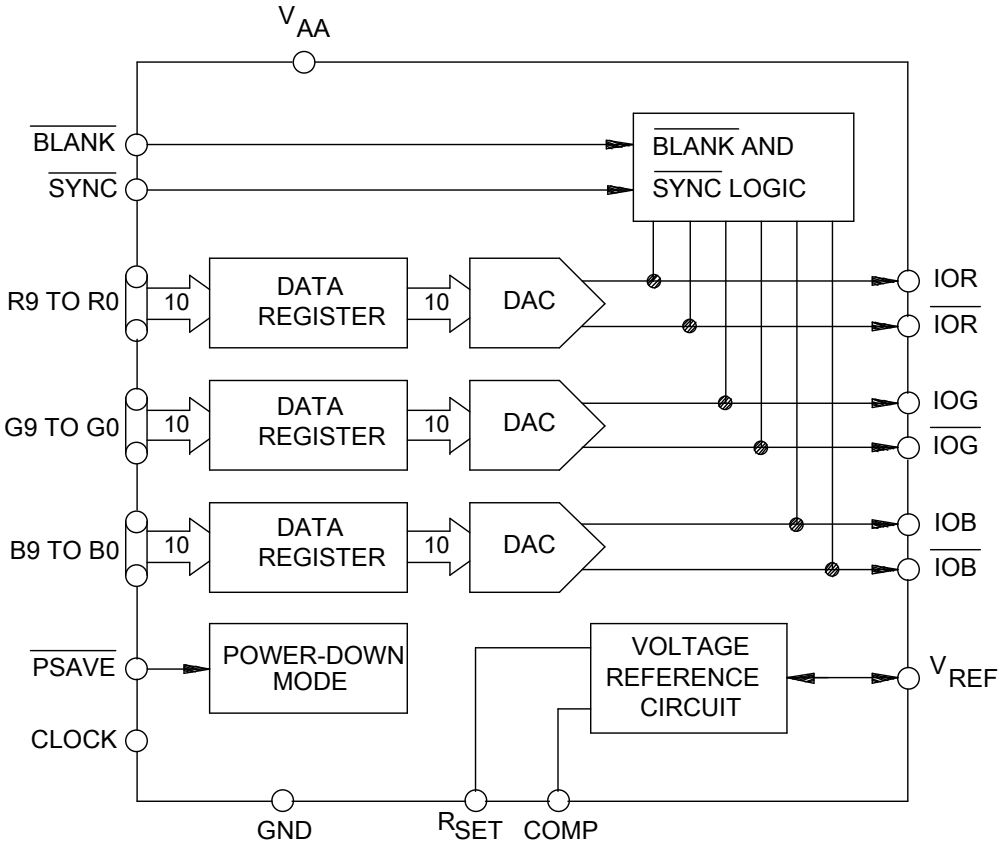
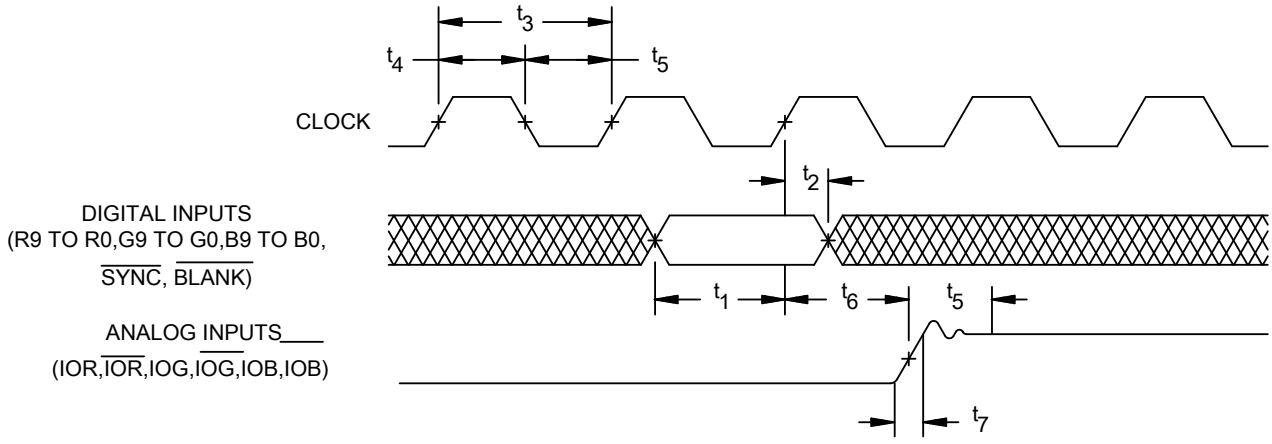


FIGURE 4. Functional block diagram.



NOTES:

1. Output delay (t_6) measured from the 50% point of the rising edge of clock to the 50% point of full scale transition.
2. Output Rise/Fall time (t_7) measured between the 10% and 90% points of full scale transition.
3. Transition time (t_8) measured from the 50% point of full scale transition to within 2% of the final output value.

FIGURE 5. Timing diagram.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number
V62/12637-01XB	24355	ADV7123SCP170EP-RL

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
24355	Analog Devices 1 Technology Way P.O. Box 9106 Norwood, MA 02062-9106